second output strobe signal are transmitted in synchronism with output data from said memory device in a [the] data output operation, the first and second output strobe signals being in complementary relation to each other, each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data.

8 16. (Amended) An electronic instrument comprising:

a memory device; and

strobe signal lines through which a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to said memory device in a [the] data input operation, the first and second input strobe signals being in complementary relation to each other, each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of the input data.

15 19. (Amended) An electronic instrument comprising:

a memory device; and

strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted in synchronism with output [out put] data from said memory device in a data output operation and a first input strobe signal and a second input strobe signal are transmitted in synchronism with input data supplied to said memory device in a data input operation, the first and second output strobe signals being in complementary relation to each other, each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data, the first and second input strobe signals being in complementary relation to each other, each of cross points of the first and second input strobe signals being set at an edge trigger point or a center point of a corresponding data item of the input data.

21 25. (Amended) A semiconductor memory device [provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation for said semiconductor memory

device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted to be used to settle output data from said semiconductor memory device in the data output operation, the first and second output strobe signals being in complementary relation to each other, said semiconductor memory device] comprising:

a data output buffer that outputs [the] output data to an exterior of said memory device [from a memory bank]; and

a strobe output buffer that generates [the] first and second output strobe signals, and outputs the first and second output strobe signals to the exterior of said memory device in synchronism with the outputting the of the output data, the first and second output strobe signals being in complementary relation to each other with each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data [based on a predetermined signal, the first and second output strobe signals being supplied from said strobe output buffer to said strobe signal lines when the output data is output from said data output buffer].

a4 cont

26. (Amended) A semiconductor memory device [provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data input operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal and a second output strobe signal are transmitted to be used to settle input data supplied to said semiconductor memory device in the data input operation, the first and second input strobe signals being in complementary relation to each other, said semiconductor memory device] comprising:

a strobe input buffer that receives [the] first and second input strobe signals from an exterior of said memory device [transmitted through said strobe signal lines] and generates a strobe clock signal based on the first and second input strobe signals, the first and second input strobe signals being in complementary relation to each other with each of cross points of the first and second input strobe signals being set at an edge trigger

point or a center point of a corresponding data item of input data; and

a data input buffer that latches the [receives] input data [items] supplied from the exterior of [to] said semiconductor memory device at such latch timings as defined by the strobe clock signal [, the input data items being settled by using the clock strobe signal generated by said input strobe buffer].

23 27. (Amended) A semiconductor memory device [provided in an electronic instrument having clock lines through which complementary clock signals are transmitted to be used for synchronization of a data output operation and a data input operation for said semiconductor memory device, and strobe signal lines through which a first output strobe signal, a second output strobe signal, a first input strobe signal and a second input strobe signal are transmitted to be used to settle output data from said memory device in the data output operation and to settle input data supplied to said semiconductor memory device, the first and second output strobe signals being in complementary relation to each other, the first and second input strobe signals being in complementary relation to each other, said memory device] comprising:

a data output buffer that outputs [the] output data to an exterior of said memory device [from a memory bank];

a strobe output buffer that generates [the] first and second output strobe signals, and outputs the first and second output strobe signals to the exterior of said memory device in synchronism with the outputting of the output data, the first and second input strobe signals being in complementary relation to each other with each of cross points of the first and second output strobe signals being set at an edge trigger point or a center point of a corresponding data item of the output data [based on a predetermined signal, the first and second output strobe signals being supplied from said strobe output buffer to said strobe signal lines when the output data is output from said data output buffer];

a4 cont.

a strobe input buffer that receives [the] first and second input strobe signals from an exterior of said memory device [transmitted through said strobe signal lines] and generates a strobe clock signal based on the first and second input strobe signals, the first